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10/777,662	02/13/2004	Makoto Ogawa	12377/5	5641

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EXAMINER	
PATEL, JAYESH A	
ART UNIT	**PAPER NUMBER**
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,662	OGAWA ET AL.	
	Examiner	Art Unit	
	Jayesh A. Patel	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

In response to applicant's arguments on **(Page 5 Line 17,Page 6 lines 9-10 and 27)** that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies **(i.e. "within each of a plurality of memory units")** are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant's arguments on **(Page 7 lines 1-2)** which states that Fujita does not disclose **"the structure in which the first, second and the third memories are comprised in each of the memory units"** the examiner disagrees. Fujita in **(Fig 10)** clearly shows the above structure.

1) Element 101 is a memory unit array.

2) Each **(2X2 blocks in bold)** are memory units in the memory unit array 101.

3) Each **(2X2 blocks in bold)** has **(circled cells 1,2,3 and 4)** which are a first memory cell, second memory cell, third memory cell and the fourth memory cell respectively.

The applicant's arguments on (Page 6 Lines 13 –14 and 20-21) **"which states complicated transferring processing is inevitable in processing data... at column and row.."** , the examiner disagrees. Fujita in the abstract discloses executing calculation at high speed in an LSI by **"constituting**

memories" and plural processors on the same LSI. Fujita further discloses this in the **"Effect of the invention"** section of the reference.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujita Yoshihiro (05-053898) hereafter Fujita in view of Kobayashi et al. (US 4550437) hereafter Kobayashi.

1. Regarding Claim 1, Fujita discloses an image processing device in **(Drawings 1- 10)** to multiply a two-dimensional pixel data by a matrix of coefficients and filter said pixel data based on a sum of the multiplied results, said image processing device comprising: a memory unit array **(Element 101 Drawing 10)** in which a plurality of memory units in a form of matrix are arranged **(2X2 blocks in bold are memory units in Drawing 10)** which at least includes a first memory cell **(circled Element 1 in each 2X2 block Drawing 10)**, a second memory cell **((circled Element 2 in each 2X2 block Drawing 10))** and a third memory cell **((circled Element 3 in each 2X2 block Drawing 10))** to store said pixel data; a

first calculator arranged in rows of and in the number of columns of, said memory unit array to perform computation of the pixel data of a specified column **(Element 21 Drawing 1)** in the memory unit array and obtain a first processing data to store in said second memory cell **(Element 102 Drawing 10)**; and a second calculator arranged in columns of, and in the number of rows of, the memory unit array to perform computation of the first processing data of a specified row **(Element 15 Drawing 1)** of the memory unit array and obtain a second processing data to store in said third memory cell **(Element 103 Drawing 10)**;

Fujita is silent and does not disclose wherein said filtering is performed based on a computed result by the second calculator. Kobayashi discloses the filtering in **(Fig 2 and Col 2 Lines 47-59)**. Kobayashi discloses a parallel processing of the image data that achieves faster processing and can be implemented in an LSI structure in **(Figs 2-5 and Col 1 Lines 30-54)**. Kobayashi further discloses processor with the spatial filter for noise removal implemented in the form of LSI at **(Col 1 Lines 10-29)**. Both Fujita and Kobayashi are from the same field of endeavor and are analogous art, therefore it would have been obvious for one of ordinary skill in the art, at the time the invention was made to use the teachings of Kobayashi of parallel processing and (spatial filter) in the apparatus of Fujita for the above reasons.

2. Regarding Claim 2, Fujita and Kobayashi discloses the image processing

device according to claim 1. Fujita further discloses wherein said first processing data is stored in a memory unit located in a middle row among said memory units in the specified column **(Drawing 10 element 102)**, and said second processing data is stored in a memory unit in a middle column among said memory units in the specified row in **(Drawing 10 Element 103)**.

3. Claim 3 is a corresponding method claim of a device of Claim1. See the explanation of Claim 1.

4. Regarding claim 4, Fujita and Kobayashi discloses the image processing method according to claim 3. Fujita further discloses wherein said first processing data is stored in the memory unit in the middle row among said memory units in the specified column, and said second processing data is stored in the memory unit in the middle column among said memory units in the specified row in **(Drawing 10 Elements 102 and 103)**. Fujita further discloses this in **(Para 0022,0023,0024 and 0025)** of the detailed description.

5. Regarding Claim 5, Fujita and Kobayashi discloses the image processing method according to claim 3. Fujita further discloses wherein computation in said first step is performed by shifting along rows, and subsequently, computation in said second step is performed by shifting along columns in **(Drawing 3 and Para 0031-0035 of the Detailed Description)**. Drawing 10 also discloses the transfer

and computation of the pixel data at **(Para 0022-0026)**. Kobayashi also discloses the computation and shifting in **(Figs 4,5 and Col 3 Lines 22-67 through Col 4 Lines 1- 15)**.

6. Regarding Claim 6, Fujita and Kobayashi discloses the image processing method according to claim 4. Fujita further discloses wherein computation in the first step is performed by shifting along rows, and subsequently, computation in the second step is performed by shifting along columns at **(Drawing 3 and Para 0031-0035 of the Detailed Description)**. Drawing 10 also discloses the transfer and computation of the pixel data at (Para 0022-0026). Kobayashi also discloses the computation and shifting in **(Figs 4,5 and Col 3 Lines 22-67 through Col 4 Lines 1- 15)**.

7. Regarding Claim 7, Fujita and Kobayashi disclose the image processing method according to claim 3. Fujita further disclose wherein computation in the second step is performed by shifting along columns, and subsequently, computation in the first step is performed by shifting along rows at **(Drawing 3 and Para 0031-0035 of the Detailed Description)**. Drawing 10 also discloses the transfer and computation of the pixel data at (Para 0022-0026). Kobayashi also discloses the computation and shifting in **(Figs 4,5 and Col 3 Lines 22-67 through Col 4 Lines 1- 15)**.

8. Regarding Claim 8, Fujita and Kobayashi discloses the image processing method according to claim 4. Fujita further disclose wherein computation in the second step is performed by shifting along columns, and subsequently, computation in the fist step is performed by shifting along rows at **(Drawing 3 and Para 0031-0035 of the Detailed Description)**. Drawing 10 also discloses the transfer and computation of the pixel data at (Para 0022-0026). Kobayashi also discloses the computation and shifting in **(Figs 4,5 and Col 3 Lines 22-67 through Col 4 Lines 1- 15)**.

Conclusion

Examiner cites particular columns and line numbers in the references as applied to the claims below for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed

within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jayesh A. Patel whose telephone number is 571-270-1227. The examiner can normally be reached on M-F 7.00am to 4.30 pm (5-4-9). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on 571-272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service

Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jayesh Patel
08/24/07
JP

JINGGE WU
SUPERVISORY PATENT EXAMINER